3-08-04 Image AF/2814

Express Mail Label No. EV443088297US

PATENT APPLICATION
Docket No. 11675.76.1.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:	Gurtej Sandhu et al.	Art Unit
Serial No.:	09/627,381	2814
Filed:	July 28, 2000	
Confirmation No.:	2473	
For:	INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME	
Examiner:	Tuan Quach	

CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10

I hereby certify that the following documents are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 5th day of March 2004.

- Appeal Brief of Appellant
- Check No. 135849 for $330.00
- Transmittal Letter
- Postcard

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellants
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\76.1.1\VFW0000003112V001.doc

Express Mail Label No. EV443088297US

PATENT APPLICATION
Docket No. 11675.76.1.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:		
	Gurtej Sandhu et al.	
		Art Unit
Serial No.:	09/627,381	2814
Filed:	July 28, 2000	
Confirmation No.:	2473	
For:	INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME	
Examiner:	Tuan Quach	

TRANSMITTAL OF APPEAL BRIEF UNDER 37 C.F.R. § 1.192

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is a Brief of Appellant for entry in the above-identified application. Appellant has filed a timely Notice of Appeal from the action of the Examiner dated July 3, 2003. Also enclosed are the following:

x A Certificate of Express Mail Under 37 C.F.R. § 1.10

x Check No. 135849 in the amount of $330.00 for the filing fee.

---

x The Commissioner is hereby authorized to charge payment of any patent application processing fees under 37 CFR 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-3178. Duplicate copies of this sheet are attached.

Dated this 5th day of March 2004.

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellants
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\76.1.1\VFW0000003112V001.doc

Express Mail Label No. EV443088297US

PATENT APPLICATION
Docket No. 11675.76.1.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:	Gurtej Sandhu et al.	Art Unit
Serial No.:	09/627,381	2814
Filed:	July 28, 2000	
Confirmation No.:	2473	
For:	INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME	
Examiner:	Tuan Quach	

BRIEF OF APPELLANT

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants, Gurtej Sandhu et al., have filed a timely Notice of Appeal from the action of the Examiner in rejecting pending claims 1-35, 37, and 38 in this application in the Office Action dated July 3, 2003. This brief is being filed under the provisions of 37 C.F.R. § 1.192. The filing fee of $330.00, as set forth in 37 C.F.R. § 1.17(c) is submitted herewith.

REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., by way of assignment from Gurtej Sandhu, Anand Srinivasan, and Ravi Iyer, who are the named inventors in the present application. The assignment documents were recorded at Reel No. 8109, Frame 0517 in the United States Patent and Trademark Office on July 10, 1996.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-35, 37 and 38 are pending and appealed in the present application. Claim 36 has been cancelled.

STATUS OF AMENDMENTS

All amendments have been previously entered.

SUMMARY OF INVENTION

The present invention is directed to a method of forming an interlevel dielectric comprising providing a first dielectric layer 14 over a surface of a substrate 12 situated on a semiconductor wafer, depositing a conductive layer 34 on the first dielectric layer, with the conductive layer having an upper surface and a lower surface, and depositing an additional layer 36 on the conductive layer (*see* Fig. 3, Spec. pp. 10-11). The conductive layer and the additional layer are patterned by forming a patterned mask layer on the additional layer, and etching

through the additional layer and the conductive layer and into the first dielectric layer, leaving a space between adjacent remaining portions of the conductive layer, the adjacent remaining portions of the conductive layer forming lines of conductive material. A layer of dielectric material 17 having a dielectric constant of less than about 3.6 is deposited to fill the space. The layer of dielectric material extends above the upper surface of the adjacent lines of conductive material and below the lower surface of the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween, but does not extend directly over or under the upper and lower surfaces of the adjacent lines of conductive material. The layer of dielectric material is removed from the top thereof downward to at least the level of the top of the additional layer. A second dielectric layer 21 is deposited over all layers on the surface of the substrate (*see* Fig. 4).

ISSUES

1. Whether claims 1-10 are unobvious over U.S. Patent No. 5,445,996 to Kodera et al. (hereinafter "*Kodera*") taken with U.S. Patent No. 5,708,303 to Jeng (hereinafter "*Jeng* '303"), U.S. Patent No. 5,486,493 to Jeng (hereinafter "*Jeng* '493"), and U.S. Patent No. 5,641,382 to Shih et al. (hereinafter "*Shih*").

2. Whether claims 11-35, 37, and 38 are unobvious over *Kodera*, taken with *Jeng* '303, *Jeng* '493, and *Shih*.

GROUPING OF CLAIMS

Claims 1-10 stand or fall together. Claims 11-24, 28-33, 35, 37, and 38 stand or fall together. Claim 25 stands or falls alone. Claim 26 stands or falls alone. Claim 27 stands or falls alone. Claim 34 stands or falls alone. Claim 35 stands or falls alone.

ARGUMENT

1. Claims 1-10 are Unobvious Over *Kodera* Taken With *Jeng* '303, *Jeng* '493, and *Shih*

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kodera* taken with *Jeng* '303, *Jeng* '493, and *Shih*. For the reasons that follow, Appellants respectfully submit that claims 1-10 are unobvious over the cited references.

The law is well settled that to "establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation ... to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (citations omitted) M.P.E.P. §§ 2142, 2143, p. 2100-121, -122, 8th ed. (Aug. 2001).

Claim 1 recites, *inter alia*, "the layer of dielectric material extending above the upper surface of the adjacent lines of conductive material and below the lower surface of the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween, but not

extending directly over or under the upper and lower surfaces of the adjacent lines of conductive material." None of *Kodera*, *Jeng* '303, *Jeng* '493, or *Shih* teaches or suggests this limitation.

In particular, Appellants submit that the rejection of claims 1-10 fails to give proper weight to a solution recited by claim 1 - the reduction of fringe capacitance. As stated in the present application with respect to the problem of fringe capacitance that is overcome by the present invention:

> The electric field formed by a potential difference applied across an adjacent pair of lines of conductive material 16 is strongest in a direct line and centrally between the adjacent pair, such as along dashed line N in Figure 2. But the electric field so formed also extends to a fringe area not in a direct line between the adjacent pair, such as along dashed line F in Figure 2. The field in this area, called the fringe, is associated with a portion of the total capacitance, the portion called herein "fringe capacitance," between the adjacent pair.

Specification at page 10, lines 6-11. In order to overcome the above problem of fringe capacitance, both above and below a direct line between the paired lines of conductive material, the present invention extends the low dielectric constant material both above and below the upper and lower surface of the paired lines of conductive material. In order to accomplish the low dielectric constant material layer extending below the bottom layer of each conductive line, the step of etching requires: "etching through said additional layer and said conductive layer and into said first dielectric layer," as recited in claim 1.

In contrast, *Kodera* does not teach a dielectric material layer extending below the bottom surface of a conductive layer, does not teach the use of low dielectric constant materials, does not address the problem of fringe capacitance, and in fact clearly illustrates a failure to comprehend, appreciate, or design for a solution to the problem of fringe capacitance. *Kodera* teaches, as seen in Figure 30C, a dielectric material 217 in spaces between adjacent conductive material 222 that

has a top surface that is above the top surface of the conductive material 222 and a bottom surface that is on the same level with the bottom surface of conductive material 222. Again, *Kodera* also teaches, as seen in Figure 33J, a dielectric material 246 in spaces between adjacent conductive material 203 that has a top surface that is above the top surface of conductive material 203 and a bottom surface that is on the same level with the bottom surface of conductive material 203.

These two examples clearly illustrate that *Kodera* does not teach or suggest a solution to the problem of fringe capacitance. Rather, *Kodera* seeks to improve a polishing operation on the upper surface of the dielectric layers 217, 246. In particular, *Kodera* uses a spacer layer to create a polishing stop. Although this creates a final product with a dielectric layer that extends higher than the adjacent conductor layer, this does not address the problem of fringe capacitance. When the structures taught by *Kodera* are compared to Figure 2 of the present application, the differences are pronounced. For example, reference numeral F within dielectric material 17 in Figure 2 of the present application illustrates a solution produced by the inventive method that is not taught, suggested, or implied by the teachings of *Kodera*.

Neither of *Jeng* '303 or *Jeng* '493 (the "*Jeng* patents") are properly combinable with *Kodera* to obviate the presently recited claims. In particular, the methods disclosed in the *Jeng* patents and *Kodera* are diametrically opposite. The *Jeng* patents involve reduction of cross talk using a damascene process where the dielectric is first deposited (low dielectric constant or otherwise) and the dielectric trenches are then etched where the metal is to be deposited. In contrast, *Kodera* involves an improved polishing method using the process of forming metal lines first and then putting the dielectric in between the metal lines. Hence, there would have

been no motivation for one skilled in the art practicing *Kodera* to look to the teachings of the *Jeng* patents.

In addition, neither of the *Jeng* patents teach or suggest the method of claim 1 addressing the problem of fringe capacitance. Although both references acknowledge the use of low dielectric constant dielectric materials, they do not teach or suggest extending a low dielectric constant dielectric layer above and below the upper and lower surfaces of adjacent conductive lines to reduce fringe capacitance.

Finally, *Shih* is cited for disclosing etching below the lower surface of adjacent conductive lines. Applicants respectively assert that *Shih* in fact expressly teaches away from any motivation to do so:

> [T]he etching time used to form the electrode pattern 15 can be increased to remove the silicon nodules but this will result in over etched regions 18 of the dielectric layer 12 and deterioration of the photoresist pattern 16 used to form the electrode pattern. The deterioration of the photoresist pattern can cause loss of photoresist at the pattern edge 17 resulting in a less desirable electrode cross section profile.

Shih at column 1, lines 57-64. Thus, while *Shih* acknowledges that is known to inadvertently overetch adjacent to conductive lines as part of the process to remove silicon nodules, the practice is clearly discouraged because of its associated problems of overetched regions of dielectric layers and loss of photoresist at the pattern edge. Therefore, the expressly acknowledged deficiencies of overetching in *Shih* would not provide any motivation to modify *Kodera* by combining the teachings of *Kodera* and *Shih* to overetch silicon dioxide layer 202 in *Kodera.*

Claims 2-10 depend from claim 1, include the limitations thereof, and are therefore patentable over the cited references for at least the foregoing reasons presented hereinabove with respect to claim 1.

Accordingly, Appellants submit that claims 1-10 would not have been obvious over *Kodera*, taken with *Jeng* '303, *Jeng* '493, and *Shih*.

2. Claims 11-35, 37 and 38 are Unobvious Over *Kodera* Taken With *Jeng* '303, *Jeng* '493, and *Shih*

Independent claims 11 and 35 recite "leaving a space between adjacent remaining portions of said conductive layer that *extends below the lower surface of said conductive layer*" (emphasis added). Independent claims 34 and 35 recite similar limitations.

In contrast, *Kodera* does not teach such recited features. Rather, *Kodera* teaches a dielectric material 217 in spaces between adjacent conductive material 222 that has a top surface that is above the top surface of the conductive material 222 and a bottom surface that is on the same level with the bottom surface of conductive material 222 (Figure 30C). *Kodera* also teaches a dielectric material 246 in spaces between adjacent conductive material 203 that has a top surface that is above the top surface of conductive material 203 and a bottom surface that is on the same level with the bottom surface of conductive material 203 (Figure 33J).

As discussed previously, neither of the *Jeng* patents are properly combinable with *Kodera* to obviate the presently recited claims, since the methods of the *Jeng* patents and *Kodera* are diametrically opposite. The *Jeng* patents use a damascene process where the dielectric is first deposited and dielectric trenches are then etched where the metal is to be deposited. In contrast, *Kodera* uses the process of forming metal lines first and then putting the dielectric in between the metal lines. Also, the expressly acknowledged deficiencies of overetching in *Shih* as discussed above would not provide any motivation to modify *Kodera* by combining the teachings of *Kodera* and *Shih*.

In addition, independent claim 11 recites, *inter alia*:

> patterning said conductive layer by:
> forming a mask layer on said conductive layer; and
> etching through said conductive layer and into said first dielectric layer, . . . ;
>
> depositing an additional layer on the upper surfaces of lines of conductive material and on said first dielectric layer;

Independent claim 22 recites, *inter alia*:

> patterning said metal layer by:
> forming a mask layer on said metal layer; and
> etching through said metal layer and into said first dielectric layer, . . . ;
>
> depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;

Kodera does not teach or suggest such recited features. Rather, *Kodera* forms a polysilicon wiring film 203, forms a carbon film 244 over polysilicon wiring film 203, forms a photoresist layer 245 over carbon film 244, and then sequentially etches carbon layer 244 and polysilicon wiring film 203. *Jeng* '303, *Jeng* '493, and *Shih* do not address the formation of an additional layer and therefore cannot overcome the deficiencies of *Kodera* in any combination therewith to teach or suggest the recited limitations of claims 11 and 22.

Claims 12-21, 23-33, 37, and 38 depend from either claim 11 or claim 22, include the limitations thereof, and are therefore patentable over the cited references for at least the foregoing reasons with respect to claims 11 and 22.

Additionally, claims 25-27 recite additional limitations not taught or suggested by the cited references. These include, for example: "etching said additional layer" (claim 25); "wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer" (claim 26); and "wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine

based plasma (claim 27)."

Finally, claim 35 also recites, "etching through said additional layer and said conductive layer in a single etch step." Because *Kodera* uses a carbon film 244, separate etch steps are required, using O_2 and CF_4 (*Kodera*, column 31, lines 58-64). Therefore, *Kodera* does not teach or suggest this limitation of claim 35.

Accordingly, Appellants submit that claims 11-35, 37, and 38 would not have been obvious over *Kodera*, take with *Jeng* '303, *Jeng* '493 and *Shih*.

3. Rejection Under the Judicially Created Doctrine of Double Patenting

Claims 1-35 have been rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-32 of U.S. Patent No. 6,107,183 to Sandhu et al.

Appellants are willing to submit a terminal disclaimer once allowable subject matter is indicted for any of claims 1-35 of the present application.

In view of the foregoing, Appellants respectfully request the Board to overturn the Examiner's rejections of the appealed claims.

Dated this 5th day of March 2004.

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellants
Registration No. 34,263
Customer No. 022901

GMT:vfw
G:\DATA\WPDOCS\VFW\GMT\116757611:appealbrief.doc

APPENDIX: CLAIMS ON APPEAL

1. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer, the conductive layer having an upper surface and a lower surface;

depositing an additional layer on said conductive layer;

patterning said conductive layer and said additional layer by:

forming a patterned mask layer on said additional layer; and

etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the adjacent lines of conductive material and below the lower surface of the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween, but not extending directly over or under the upper and lower surfaces of the adjacent lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

2. The method as defined in Claim 1, further comprising the step, to be performed after said step of removing said layer of dielectric material and before said step of depositing a second dielectric layer, of removing said additional layer on said lines of conductive material.

3. The method as defined in Claim 2, wherein said additional layer comprises titanium.

4. The method as defined in Claim 2, wherein said additional layer comprises TiN.

5. The method as defined in Claim 1, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

6. The method as defined in Claim 1, wherein said dielectric material comprises PTFE.

7. The method as defined in Claim 1, wherein said additional layer comprises silicon dioxide.

8. The method as defined in Claim 1, wherein said step of removing said layer of dielectric material comprises an etch back step.

9. The method as defined in Claim 1, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

10. The method as defined in Claim 1, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, copper, tungsten, and multiple layers of TiN/Al/TiN, TiN/Al/Ti, W/TiN/Ti, or any combinations thereof.

11. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer, the conductive layer having a lower surface and an upper surface;

patterning said conductive layer by:

forming a mask layer on said conductive layer; and

etching through said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material each having an upper surface;

depositing an additional layer on the upper surfaces of lines of conductive material and on said first dielectric layer;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

12. The method as defined in Claim 11, wherein depositing an additional layer comprises depositing a layer of silicon dioxide by silane and oxygen based plasma enhanced chemical vapor deposition.

13. The method as defined in Claim 11, further comprising, after depositing an additional layer and before depositing a layer of dielectric material, of etching said additional layer.

14. The method as defined in Claim 13, wherein said additional layer has a top surface extending to a lateral surface at a corner, and wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer.

15. The method as defined in Claim 13, wherein said additional layer comprises silicon dioxide and wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine based plasma.

16. The method as defined in Claim 11, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

17. The method as defined in Claim 11, wherein said dielectric material comprises PTFE.

18. The method as defined in Claim 11, wherein said additional layer comprises silicon dioxide.

19. The method as defined in Claim 11, wherein said step of removing said layer of dielectric material comprises an etch back step.

20. The method as defined in Claim 11, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

21. The method as defined in Claim 11, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, and copper.

22. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a metal layer on said first dielectric layer, the metal layer having a lower surface and an upper surface;

patterning said metal layer by:

forming a mask layer on said metal layer; and

etching through said metal layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said metal layer that extends below the lower surface of said metal layer, said adjacent remaining portions of said metal layer forming metal lines each having an upper surface;

depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space, the layer of dielectric material extending above the upper surface of the lines of conductive material and below the lower surface of the lines of conductive material but not directly over or under the upper and lower surfaces of the lines of conductive material;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

23. The method as defined in Claim 22, wherein said step of depositing a layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines comprises an ozone-based TEOS deposition.

24. The method as defined in Claim 22, wherein said metal lines comprise aluminum with a titanium nitride film on said upper surface of said metal lines.

25. The method as defined in Claim 22, further comprising, after depositing a layer of silicon dioxide conformably over said metal lines and before depositing a layer of dielectric material, of etching said additional layer.

26. The method as defined in Claim 25, wherein said additional layer has a top surface extending to a lateral surface at a corner, and wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer.

27. The method as defined in Claim 26, wherein said additional layer comprises silicon dioxide and wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine based plasma.

28. The method as defined in Claim 22, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

29. The method as defined in Claim 22, wherein said dielectric material comprises PTFE.

30. The method as defined in Claim 22, wherein said additional layer comprises silicon dioxide.

31. The method as defined in Claim 22, wherein said step of removing said layer of dielectric material comprises an etch back step.

32. The method as defined in Claim 22, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

33. The method as defined in Claim 22, wherein said metal layer comprises at least one of aluminum or copper.

34. A method of forming an interlevel dielectric comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface and an upper surface;

forming an additional layer on said conductive layer;

forming lines of conductive material having spaces therebetween that extend below the lower surface of said conductive layer from the conductive layer;

filling the spaces between the lines of conductive material with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer, wherein said second dielectric layer and said additional layer are formed of the same material;

wherein portions of the dielectric material having a dielectric constant of less than about 3.6 extend both above and below the adjacent lines of conductive material but do not extend directly over or under the upper and lower surfaces of the lines of conductive material.

35. A method of forming an interlevel dielectric that reduces fringe capacitance between adjacent lines of conductive material, the method comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface;

forming an additional layer on said conductive layer;

etching through said additional layer and said conductive layer in a single etch step and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

filling the spaces between adjacent remaining portions of said conductive layer with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer, wherein said second dielectric layer and said additional layer are formed of the same material;

wherein the dielectric material having a dielectric constant of less than about 3.6 extends both above and below, but not directly over, the respective adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween.

37. The method as defined in Claim 11, wherein the layer of dielectric material having a dielectric constant of less than about 3.6 extends both above and below the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween.

38. The method as defined in Claim 22, wherein the layer of dielectric material having a dielectric constant of less than about 3.6 extends both above and below the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween.